

Sample Test ET-DTV S14-ST

Time 120 minutes
– use of class documents allowed –

Name: _____

Percent: _____

Matr. No.: _____

Grade: _____

1	2	3	4	X	Σ
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(1) Boolean Logic

(1.1) DeMorgan Theorem

The boolean equation $y = x_1 \cdot x_2' \cdot x_3' \cdot x_4$ should be converted to OR/NOR logic by applying the DeMorgan theorem.

Draw the complete circuit diagram with OR/NOR gates.

(1.2) Duality Theorem

Apply the Duality theorem to $(x + 0) \cdot (x + 1) = x$ (assume it is correct).

Prove the equation after applying the Duality theorem.

(1.3) Logic Minimization

Find the minimum product of sums solution for the following truth table

a	b	c	y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Draw the complete circuit diagram using only NOR gates!

(1) = 8	(2) = 8	(3) = 8	(4) = 8	Σ = 32					
1.0 ≥ 29	1.3 ≥ 27	1.7 ≥ 26	2.0 ≥ 24	2.3 ≥ 23	2.7 ≥ 21	3.0 ≥ 20	3.3 ≥ 18	3.7 ≥ 17	4.0 ≥ 15

ET-DTV / ESD 2014 sample test

(1.4) Hazards

The combinational circuit $y = x_2 \cdot x_1' + x_3' \cdot x_1 \cdot x_0$ might produce erroneous output (hazard). Draw the circuit with inverters, AND and OR gates. Draw a timing diagram for the change from $x_3 = '0', x_2 = '1', x_1 = '1', x_0 = '1'$ to $x_3 = '0', x_2 = '1', x_1 = '0', x_0 = '1'$. What type of hazard occurs?

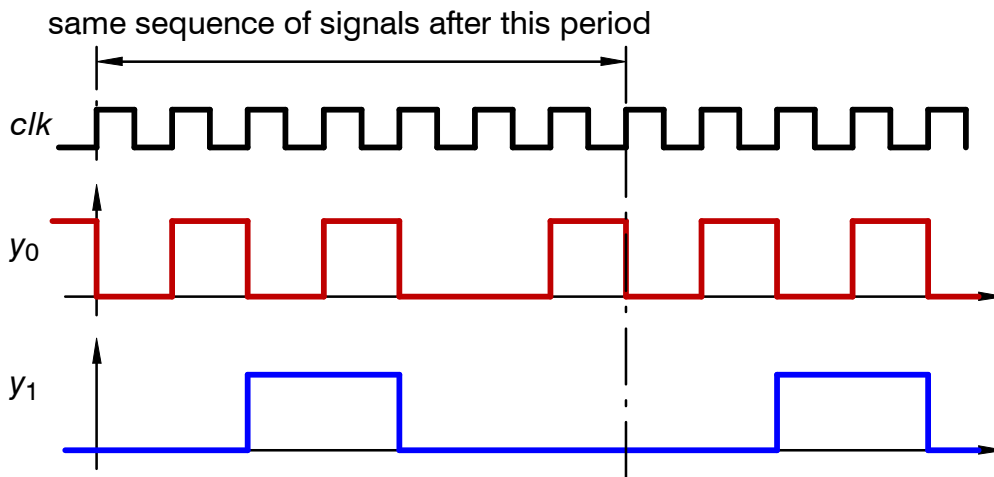
Change the design so that it becomes Hazard-free.

(2) Hardware State Machine (Moore Machine)

The following signals should be generated by a state machine with every clock cycle.

Inputs of the state machine:

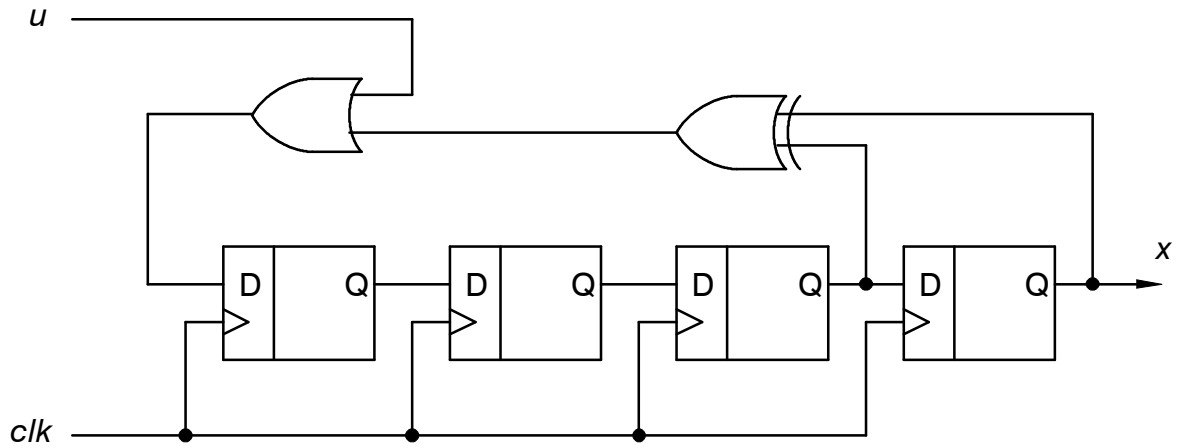
- reset* '1' => reset of the state machine, '0' operation of sm,
- start* '1' => generate sequence below, '0' => $y_0 = y_1 = '0'$.



- (2.1) How many states are required; how many flip-flops are required?
- (2.2) Draw the state diagram.
- (2.3) Design minimal solutions for the next-state logic.
- (2.4) Design minimal solution for the output logic.
- (2.5) Draw the flip-flops and output logic hardware circuit.

(3) Coupled Flip-Flops

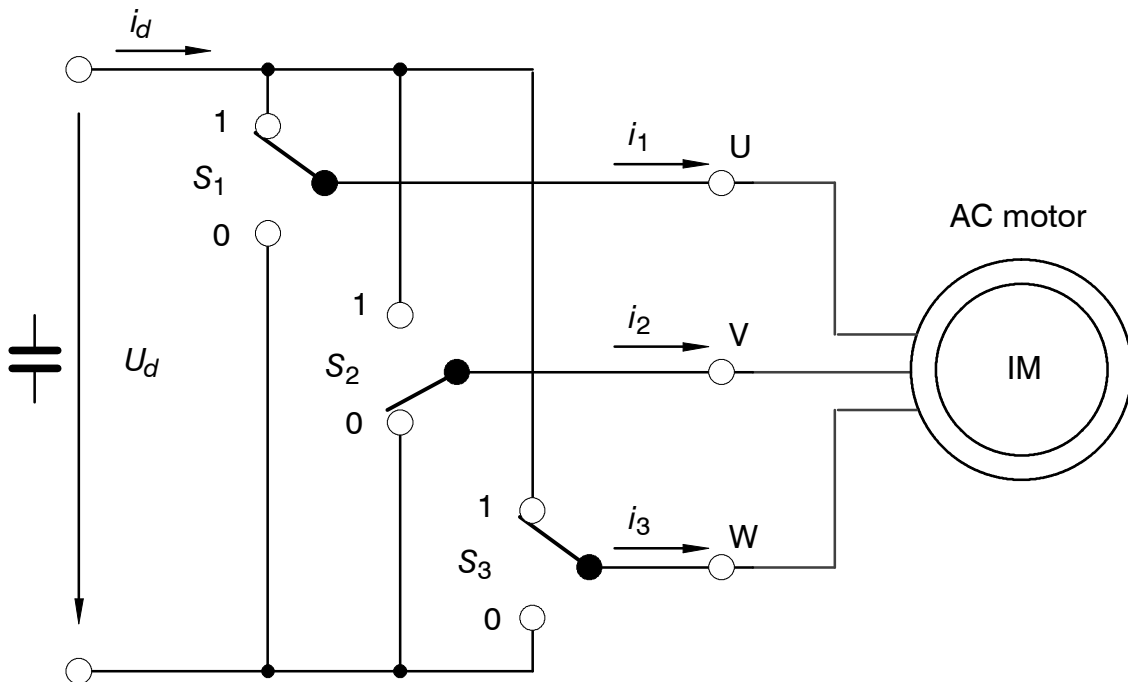
The following circuit should be synthesized by VHDL.



- (3.1) Synthesize the circuit as *structural design* in VHDL. All gates and flip-flops should be seen in the VHDL code.
- (3.2) What could be the purpose of this digital system?
- (3.3) Design the same function in a behavioral way (using a `standard_logic_vector` for all flip-flops).

(4) AC Machine Power Transistor Signals

Controlled AC drives (induction or synchronous machines) require a power inverter.



The principle of operation is shown in the above figure where pairs of power transistors are represented by switches that can be in a '0' and a '1' position. The switch position can be seen as a boolean signal.

The inverter is in “off”-state for $S_3 = S_2 = S_1 = '0'$.

Positive rotation of the machine occurs for the sequence:

<u>S3</u>	<u>S2</u>	<u>S1</u>
0	0	1
0	1	1
0	1	0
1	1	0
1	0	0
1	0	1
0	0	1
0	1	1
0	1	0
	...	
	...	

Inputs:

<code>reset</code>	'1' => resets the state machine
<code>start_stop</code>	'1' => normal (rotation) operation, '0' => “off”-state.
<code>rl_time</code>	=> determines machine frequency. This input signal is 10 bits and it determines the number of clk cycles from one switch position to the next.

- (4.1) Design a state diagram (should be consistent with your VHDL code) containing states, inputs and outputs.
- (4.2) Write a VHDL module that creates the sequence of output signals as a timed state machine. Use the `reset` and the `start_stop` and the `rl_time` signals.
- (4.3) What needs to be changed to reverse the sequence of the switches S_3 , S_2 , and S_1 ?