Hochschule Bremerhaven

INSTITUT FÜR
AUTOMATISIERUNGS-
UND ELEKTROTECHNIK

Prof. Dr.-Ing. Kai Müller

Exam Topics for ET – DTV "Digital Systems / VHDL"

- Combinational logic
  - binary operations
  - boolean expressions
  - duality theorem
  - product terms
  - minterms, maxterms
  - canonical sum, canonical product
  - circuit minimization
  - minimal realization, Karnaugh map
  - hazard and hazard avoidance
- Sequential circuits (Finite State Machines)
  - latches, and flip-flops
  - Moore and Mealy architecture
  - safe state machines (registered output)
- VHDL Elements
  - VHDL structural elements
  - intrinsic data types
  - packages and libraries
  - constants and generic mechanism
  - ports and components, instantiation of components
  - signals and attributes
  - concurrent control structures
  - sequential control structures
  - functions / procedures
  - assert functions
  - synthesizable statements and simulation constructs
  - processes
- VHDL simulation
  - functional, post synthesis and post fitting simulations
  - UUT (unit under test) setup
  - stimulus data generation with VHDL and file data
- VHDL Synthesis
  - design of combinational logic
  - design of sequential circuits and FSM
  - state diagrams and synthesis concepts
  - timed state machines

  - sequential and combinational processes for state machines
  - Digital signal processing
  - Communication protocols
    - SPI (Serial Programing Interface) master and slave receiver/transmitter
    - I2C (Inter Integrated Circuit interface) master and slave receiver/transmitter
  - I/O specifications
  - bidirectional I/O
  - design constraints (constraints file)
  - design inspection (resources, place and route)

- FPGA technology
  - LUTs, registers
  - SLICEs, SLICE types
  - switch matrix
  - clock manager
  - block RAM
  - distributed RAM
  - DSP blocks
  - programmable IO