Courses Summer Term 2020 - Kai Mueller

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Kai Mueller

Hochschule Bremerhaven / University of Applied Sciences Bremerhaven

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Thanks to James Clark, Norman Walsh and the OASIS DocBook technical committee[1].

Back to K. Mueller's Home Page[2].

[1] http://www.oasis-open.org/docbook/
[2] ../index.html

Table of Contents

1. Courses Summer Term 2020 1
2. Undergraduate Courses of Kai Mueller 2
    2.1. Digital- und Mikroprozessortechnik [ET-DMT / PMA4 und andere Bachelorstudiengänge] 2
        2.1.1. Inhalt 3
        2.1.2. Ergänzende Lehrbücher 4
    2.2. Wahlveranstaltungen im Sommersemester 2020 von Kai Müller (optional courses) 4
3. Graduate Courses of Kai Mueller 5
    3.1. Digital Systems / VHDL [ET-DTV / ESD1] 5
        3.1.1. Course contents 7
        3.1.2. Complimentary Documentation 8
    3.2. System-on-Chip Design [SY-SOC / ESD1] 9
        3.2.1. Course contents 10
        3.2.2. Complimentary Documentation 11
4. Bachelor / Master Thesis 12
5. Industriepaktika 13

List of Tables

2.1. Organisatorisches Mikroprozessortechnik 2
3.1. Organization Digital Systems / VHDL 5
3.2. Organization System-on-Chip Design 9

1

Courses Summer Term 2020

The following pages contain information on courses for the summer term 2020. Please inform me[1] *about mistakes or missing links.*

Please ignore any missing links for lab group participants. They will appear when students have registered for the lab groups during the first classes.

All informations and course documentation can be accessed on these official pages. Announcements and changes of the schedule are made *only* here.

The pages are also available for printing (PDF download)[2]. The printed version may be slightly outdated.

[1] mailto:kmueller@hs-bremerhaven.de
[2] assets/kms20.pdf

2

Undergraduate Courses of Kai Mueller

[modules for *bachelor* programs]

2.1. Digital- und Mikroprozessortechnik [ET-DMT / PMA4 und andere Bachelorstudiengänge]

==>> Dieses Modul wird empfohlen als fachliche Voraussetzung für dem Masterstudiengang ESD[1].

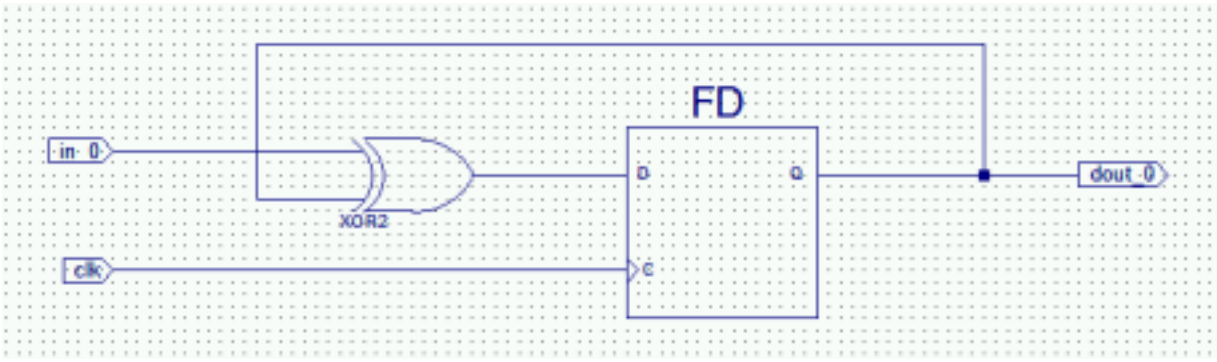


Table 2.1. Organisatorisches Mikroprozessortechnik

NEWS	Die letzte Laboraufgabe ("Motorsteuerung") ist Prüfungsleistung und wird geht mit 20% in die Bewertung der Klausur ein. Zur Klausur ist eine Programmausdruck abzugeben. Im Kopf sind Name und Matrikelnummer einzutragen. Gruppenarbeiten sind nicht zulässig, d.h. der Programmausdruck ist von jedem Teilnehmer vorzulegen.
Bemerkungen	*Wahlpflichtfach für alle technischen Studiengäge, Pflichtfach für PMA4* Nur'n paar Nullen und Einsen; einfacher kommt man nicht an eine gute Note.
Semestergruppe	PMA4, MTx, MARx, GETx, ABTx, SBTx (als Wahlpflichtfach)
Prüfung 1. Angebot	t.b.s.
Prüfung 2. Angebot	t.b.s.
Art der Lehrveranstaltung	Vorlesung 2 SWS + Labor 2 SWS

[1] http://www1.hs-bremerhaven.de/kmueller/esd/en/

Beginn	Donnerstag, 23. April 2020, 08:00h, Raum Z1090
Ende	Donnerstag, 09. Juli 2020
Termine	[Vorlesung]: Donnerstag, 1. Block/Raum Z1090 [Labor]: Donnerstag, 5. Block/Raum Z1090 (vorläufige Termine) ==> Laborplan[2]
Umdrucke	[DMT-Umdruck][3] Der Umdruck enthält die Abschnitte: 1. Digitaltechnik [Teil 1], 2. Sequenzielle Systeme [Teil 2], 3. Programmierbare Logik (CPLD, FPGA) Teil 3, 3. RISC-/CISC-CPUs, Mikroprozessoren und Mikrocontroller [Teil 4], 4. Assembler-Übungen [Teil 4], [PicoBlaze User Guide][4] © Xilinx Corp. *(neu)* *[PicoBlaze Instruction Set Summary][5] © Xilinx Corp. (wichtig)* [PicoBlaze Instruction Set Reference][6] © Xilinx Corp. (nicht ganz unwichtig)
Labore	Laborplan[7] Die letzte Laboraufgabe kann sich aufgrund neuer Laboraufbauten ändern.
Klausuren 	Übungs-Klausur mit Lösungen[8] Klausur SS03 / 1. Angebot mit Lösungen[9]
Microprozessor Interface	Schaltplan[10]
Software	Univ. Bremerhaven PicoBlaze Tools[11] (under construction)

2.1.1. Inhalt

Folgende Themen werden behandelt:

[2] assets/dmtlab42.html
[3] ../Skript/dmt_all.pdf
[4] ../VHDL/ug129.pdf
[5] ../VHDL/PB_Instr_Sum.pdf
[6] ../VHDL/PB_Instr_Ref.pdf
[7] assets/dmtlab42.html
[8] ../Klausur/pdmpss03.pdf
[9] ../Klausur/dmps031.pdf
[10] ../VHDL/DcMot_Poss.pdf
[11] http://www1.hs-bremerhaven.de/kmueller/picoblazeTools/

- Digitaltechnik:
  - Zahlendarstellung
  - Boolsche Logik
- Mikroprozessortechnik:
  - CPU-Architekturen
  - Aufbau des Mikrocontrollers 80x51
  - Instruktionssatz und Assemblerprogrammierung
  - Steuerungen und Regelungen mit Mikrocontrollern

2.1.2. Ergänzende Lehrbücher

Heesel, N. und W. Reichstein: Mikrocontroller Praxis.
Vieweg, 1996

Limbach, S.: Kompaktkurs Mikrocontroller.
Vieweg, 2002

Raisonance 80C51 and XA Development Tools Manual.
Raisonance S.A., 2000

K. Urbanski u. R. Woitowitz: Digitaltechnik.
Springer, 2000

J. Wakerly: Digital Design: Principles and Practices.
Prentice-Hall, 1999

Xilinx Vivado Users's Guide.
Xilinx Corp., 2016

2.2. Wahlveranstaltungen im Sommersemester 2020 von Kai Müller (optional courses)

Das Modul "ET-DMT" (Digital- und Mikroprozessortechnik) kann als Wahlpflichtmodul von allen technischen Studiengängen belegt werden. Beide Module sind empfohlene Voraussetzungen für den Master *ESD*.

Depending on the audience the course language will be english or german.

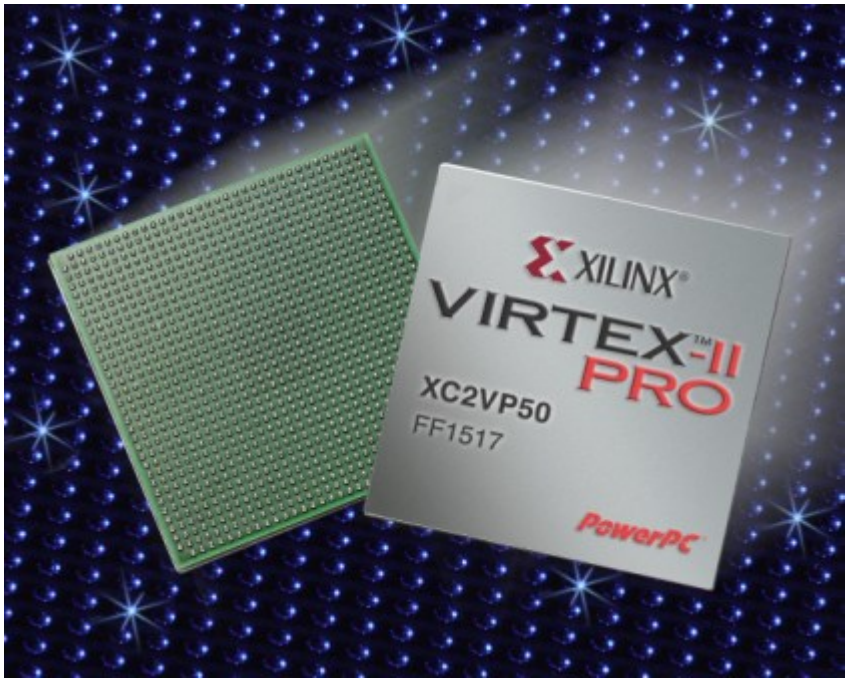
Die Wahlveranstaltungen sind für alle Studierenden der technischen Fächer geeignet.

3

Graduate Courses of Kai Mueller

[modules for *master* programs]

3.1. Digital Systems / VHDL [ET-DTV / ESD1]



© Xilinx[1]

Table 3.1. Organization Digital Systems / VHDL

NEWS	Classes and labs of this module will take place in the first half of this summer term (class 4 hours, lab 4 hours). It ends on May, 21. This module is required for SY-SOC (System-on-Chip Design) which starts on May 27 (estimated).
Study Program	Master Embedded Systems Design [ESD1]
Course Language	English
Module Description	ET-DTV[2]
Exam (1.)	- no exam -
Exam (2.)	t.b.s.

[1] http://www.xilinx.com/
[2] http://www1.hs-bremerhaven.de/kmueller/esd/esdmc/modules/ET-DTV_e.html

Credits	5
Module Type	class: 4 hours/week lab: 4 hours/week first half of summer term
Lecturer	Prof. Dr. Kai Mueller
Start of Course	Monday, April 20, 2020, *13:45h*, S316
End of Course	Wednesday, May 21, 2020 (lab)
Class/Lab Dates	==> lab group participants[3] Class #1: Monday, block 4, room S316 Class #2: Tuesday, block 3, room K02 *==> Lab participants are required to have a paper printout of the lab doc when attending the lab.* Lab Group #1: Tuesday, block 4 / 5 Lab Group #2: Wednesday, block 5 / 6 Lab Group #3: Thursday, block 3 / 4 (all labs in room Z1090)
Documents	[ESD Sample Design][4] [Complete Course Documentation][5] (updated) [FPGA Technology Basics][6] (new) This material has copyright by © Xilinx University Program, © University of Strathclyde and © Steepest Ascend Ltd, 2012 [VHDL Quick Reference][7] © Qualis Corp. [IEEE Standard Logic Quick Reference][8] © Qualis Corp.
Mandatory Lab Reports & Deadlines	For *deadlines* see lab group participants... *Report #1: Moving Light (Sequential Logic Introduction)* *Report #2: Timed state machine (Traffic Light Controller)* *Report #3: Function Generator with DAC* All designs must be synthesizable. Therefore the Synthesis Script must be part of the report (see below). Every report must contain names and matriculation numbers - group reports up to 3 students are allowed.

[3] assets/dtvlab42.html
[4] ../Skript/ESDsdex.pdf
[5] ../Skript/etdtv_all.pdf
[6] ../VHDL/FPGA_Techn.pdf
[7] ../VHDL/vhdlref.pdf
[8] ../VHDL/1164qrc.pdf

	Started : "Synthesize - XST". Running xst... Command Line: xst -intstyle ise -ifn "C:/Mue/xdev14/spirxtx/spirxtx.x Reading design: spirxtx.prj === * HDL Parsing * === Parsing VHDL file "C:\Mue\xdev14\spirxtx\spitx.vhd" into library wo Parsing entity <spitx>. Parsing architecture <Behavioral> of entity <spitx>. Parsing VHDL file "C:\Mue\xdev14\spirxtx\spirx.vhd" into library wo Parsing entity <spirx>. Parsing architecture <Behavioral> of entity <spirx>. Parsing VHDL file "C:\Mue\xdev14\spirxtx\spirxtx.vhd" into library v Parsing entity <spirxtx>. Parsing architecture <Behavioral> of entity <spirxtx>. === * HDL Elaboration * === etc... Timing Summary: --------------- Speed Grade: -3 Minimum period: 2.728ns (Maximum Frequency: 366.623MHz) Minimum input arrival time before clock: 3.567ns Maximum output required time after clock: 3.634ns Maximum combinational path delay: No path found === Process "Synthesize - XST" completed successfully
Examination Topics and Sample Test 	Test question are selected from the topics below: [Topics ET-DTV][9] Sample Test: ==>> [ET-DTV Sample Test][10] Solutions: ==>> [Sample Test Solutions][11]

3.1.1. Course contents

- Digital Systems
  - Number Systems / Codes

[9] ../Klausur/etdtv_topics.pdf
[10] ../Klausur/etdtv_st.pdf
[11] ../Klausur/etdtv_stsoln.pdf

  - Combinational Logic
  - Sequential Systems, State Machines
  - Microprocessors, RISC and CISC Architectures
  - Busses, Ports
  - CPLDs, FPGAs
- VHDL
  - Simulation and Verification of Digital Systems
  - Design of Combinational and Sequential Systems
  - Libraries
  - Intellectual Properties

3.1.2. Complimentary Documentation

K. Urbanski u. R. Woitowitz: Digitaltechnik.
Springer, 2000

J. Wakerly: Digital Design: Principles and Practices.
Prentice-Hall, 1999

J. Reichardt, B. Schwarz: VHDL-Synthese.
Oldenbourg, 2001

S. Yalamanchili: VHDL Starter's Guide.
Prentice-Hall, 1998

P. J. Ashenden: The Designer's Guide to VHDL.
Elsevier/Morgan Kaufmann, 2008

V. A. Pedroni: Circuit Design and Simulation with VHDL.
MIT Press, 2010

R. Lipsett, C. Schaefer and C. Ussery: VHDL: Hardware Description and Design.
Kluwer Academic Publishers, 1990

Xilinx Vivado Users's Guide.
Xilinx Corp., 2019

Modelsim User's Guide.
Mentor Graphics, 2010

3.2. System-on-Chip Design [SY-SOC / ESD1]

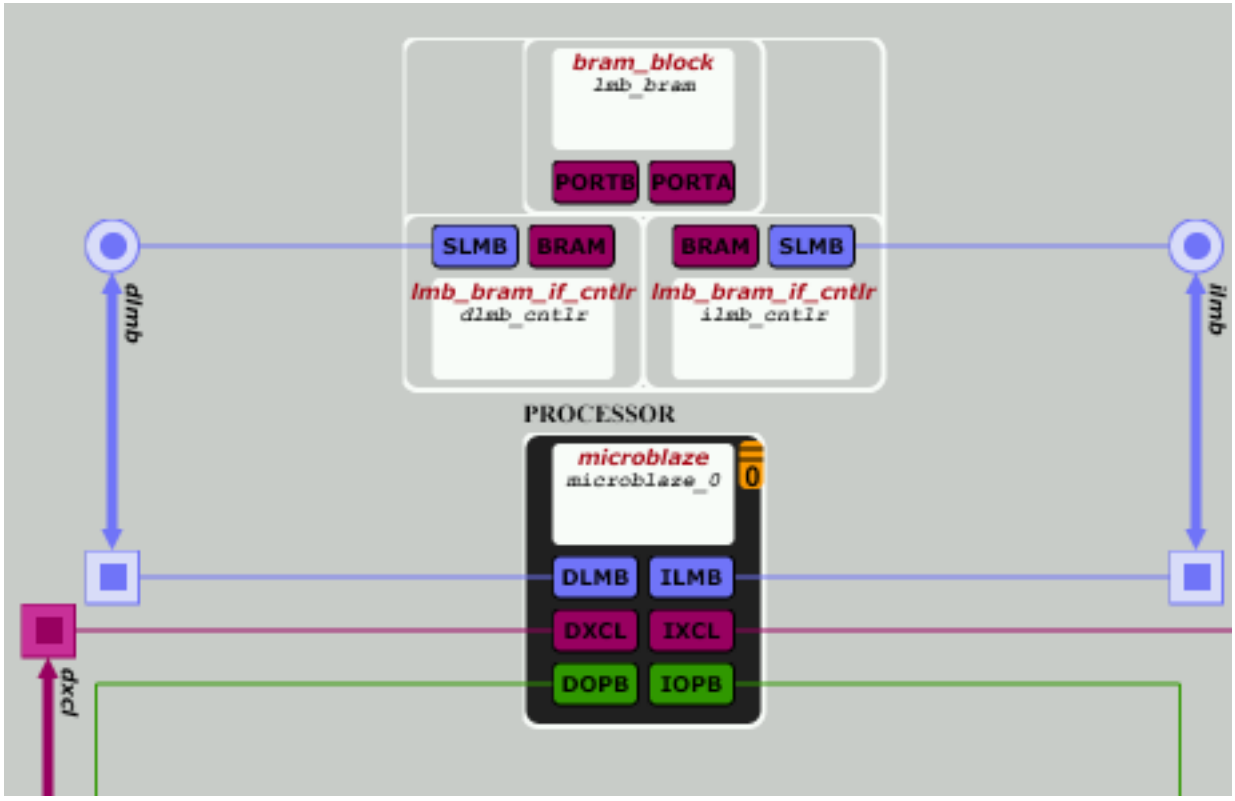


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Table 3.2. Organization System-on-Chip Design

NEWS	*Start of course is Monday, May 25, 13:45h, room S316* The module ET-DTV (Digital Systems / VHDL) is required to take this course.
Study Program	Master Embedded Systems Design [ESD1]
Course Language	English
Module Description	SY-SOC[13]
Exam (1.)	- no exam -
Exam (2.)	t.b.s.
Credits	5
Module Type	class: 4 hours/week lab: 4 hours/week second half of summer term
Lecturer	Prof. Dr. Kai Mueller
Start of Course	Monday, May 25, 2020, *13:45h*, S316
End of Course	Wednesday, July 09, 2020 (lab)
Class/Lab Dates	==> lab group participants[14]

[12] http://www.xilinx.com/
[13] http://www1.hs-bremerhaven.de/kmueller/esd/esdmc/modules/SY-SOC_e.html
[14] assets/soclab42.html

	Class #1: Monday, block 4, room S316 Class #2: Tuesday, block 3, room K02 ==> *Lab participants are required to have a paper printout of the lab doc when attending the lab.* Lab Group #1: Tuesday, block 4 / 5 Lab Group #2: Wednesday, block 5 / 6 Lab Group #3: Thursday, block 3 / 4 (all labs in room Z1090)
Mandatory Lab Reports & Deadlines	*Report #1: Discrete PI Controller (PicoBlaze)* *Report #2: Hardware accelerated DSP (Zynq)* The design must be fully synthesized. Therefore the Synthesis Script must be part of the report (see below). Every report must contain name and matriculation numbers (up to three group members).
Documents	[SY-SOC Complete Course Documentation][15] ==>> [PI controller PicoBlaze template][16] [PicoBlaze User Guide][17] © Xilinx Corp. *[PicoBlaze Instruction Set Summary][18] © Xilinx Corp. (very important)* [PicoBlaze Instruction Set Reference][19] © Xilinx Corp. (not so important)
Examination Topics and Sample Test 	Test question are selected from the topics below: [Topics ET-SOC][20] Sample Test: ==>> [SY-SOC Sample Test][21] Solutions: ==>> [Sample Test Solutions][22]

3.2.1. Course contents

- Embedded Processors
  - Microprocessor Cores in FPGAs, 8 Bits / 32 Bits
  - Software Development of Embedded CPUs

[15] ../Skript/sysoc_all.pdf
[16] assets/pi_TEMPL.psm
[17] ../VHDL/ug129.pdf
[18] ../VHDL/PB_Instr_Sum.pdf
[19] ../VHDL/PB_Instr_Ref.pdf
[20] ../Klausur/etsoc_topics.pdf
[21] ../Klausur/sysoc_st.pdf
[22] ../Klausur/sysoc_stsoln.pdf

  - Memory Interface / Memory Controllers
  - Busses
  - Interrupts
  - Real-time Scheduler, Operating Systems
- Periphery
  - A/D- and D/A-converters
  - Serial Busses
  - Ethernet and Real-time Ethernet
- Sample applications
  - Simple Industrial Control System
  - Simple Medical Device
  - Measurement System

3.2.2. Complimentary Documentation

J. Wakerly: Digital Design: Principles and Practices.
Prentice-Hall, 1999

Pong P. Chu: FPGA Prototyping By VHDL Examples
(Xilinx Spartan-3 Version)
Wiley Interscience, 2008

R. Reis, M. Lubaszewski, J.A.G. Jess: Design of Systems on a Chip: Design and Test
Springer 2010

B.M. Al-Hashimi: System-on-Chip: Next Generation Electronics (Circuits, Devices and Systems)
Instit. of Eng. and Technology, 2006

Xilinx PicoBlaze™ Users's Guide.
Xilinx Corp., 2014

Xilinx MicroBlaze™ Users's Guide.
Xilinx Corp., 2014

Modelsim User's Guide.
Mentor Graphics, 2012

4 Bachelor / Master Thesis

Bachelorarbeiten bzw. Master Thesis im Bereich Automatisierungstechnik, Regelungstechnik, Messtechnik oder Embedded Systems können können am IAE oder in der Industrie angefertigt weden.

Angebote:

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Anschrift:

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An der Karlstadt 8
27568 Bremerhaven
Tel. (0471) 4823 - 415

[1] mailto:kmueller@hs-bremerhaven.de

5 Industriepaktika

Bei der Beschaffung geeigneter Praktikantenplätze können wir Unterstützung leisten.

Anschrift:

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