# Courses Summer Term 2021 - Kai Mueller

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**Hochschule Bremerhaven / University of Applied Sciences Bremerhaven**


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Thanks to James Clark, Norman Walsh and the OASIS DocBook technical committee[1].

Back to K. Mueller's Home Page[2].

[1] http://www.oasis-open.org/docbook/
[2] ../index.html

# Table of Contents

# List of Tables

# 1

# Courses Summer Term 2021

*The following pages contain information on courses for the summer term 2021. Please inform me*[1] *about mistakes or missing links.*

*Please ignore any missing links for lab group participants. They will appear when students have registered for the lab groups during the first classes.*

All informations and course documentation can be accessed on these official pages. Announcements and changes of the schedule are made *only* here.

The pages are also available for printing (PDF download)[2]. The printed version may be slightly outdated.

[1] mailto:kmueller@hs-bremerhaven.de
[2] assets/kms21.pdf

# 2

# Undergraduate Courses of Kai Mueller

[modules for *bachelor* programs]

## 2.1. Digital- und Mikroprozessortechnik [ET-DMT / PMA4 und andere Bachelorstudi-engänge]

==>> Dieses Modul wird empfohlen als fachliche Voraussetzung für dem Masterstudiengang ESD[1].

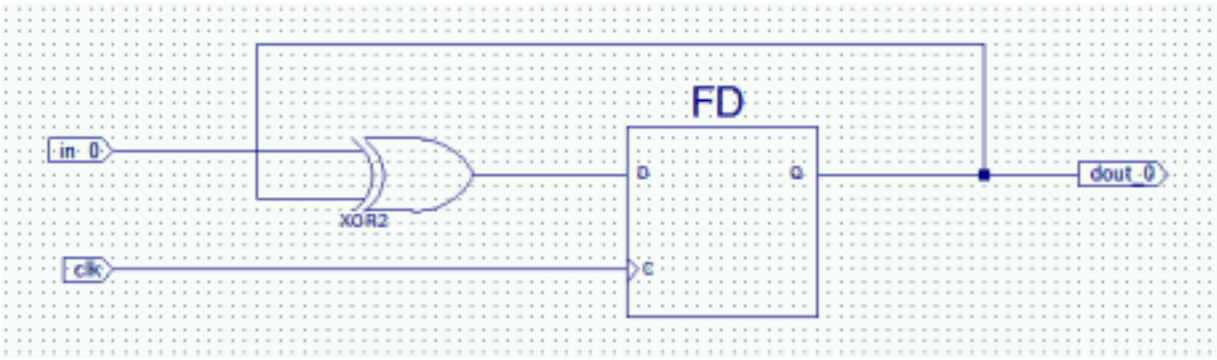



**Table 2.1. Organisatorisches Mikroprozessortechnik**

| | |
|---|---|
| *NEWS* | *Die Lehrveranstaltung findet als On-Line-Vorlesung statt!*<br><br>*Bitte auf elli[2] registrieren (unter PT S21 -> ET-DMT Digital- und Mikroprozessortechnik S21)*<br><br>Die letzte Laboraufgabe ("Motorsteuerung") ist Prüfungsleistung und wird geht mit 20% in die Bewertung der Klausur ein. Zur Klausur ist eine Programmausdruck abzugeben. Im Kopf sind Name und Matrikelnummer einzutragen. Gruppenarbeiten sind nicht zulässig, d.h. der Programmausdruck ist von jedem Teilnehmer vorzulegen. |
| Bemerkungen | *Wahlpflichtfach für alle technischen Studiengäge, Pflichtfach für PMA4*<br><br>Nur'n paar Nullen und Einsen; einfacher kommt man nicht an eine gute Note. |

[1] https://www.hs-bremerhaven.de/esd/
[2] https://elli.hs-bremerhaven.de/

| | |
|---|---|
| Semestergruppe | PMA4, MTx, MARx, GETx, ABTx, SBTx (als Wahlpflicht-fach) |
| Prüfung 1. Angebot | t.b.s. |
| Prüfung 2. Angebot | t.b.s. |
| Art der Lehrveranstaltung | Vorlesung 2 SWS + Labor 2 SWS |
| Beginn | Donnerstag, 15. April 2021, 08:30h, *Cisco WebEX (On-line)* |
| Ende | Donnerstag, 16. Juli 2021 |
| Termine | [Vorlesung]: Donnerstag, 1. Block/Raum online (Z1090)<br>[Labor ]: Freitag, 2. Block/Raum online (Z1090)<br>(vorläufige Termine) |
| Umdrucke | ==> auf elli[3] |
| Labore | ==> auf elli[4] |
|  Klausuren | Übungs-Klausur mit Lösungen[5]<br>Klausur SS03 / 1. Angebot mit Lösungen[6] |
| Microprozessor Interface | Schaltplan[7] |
| Software | Univ. Bremerhaven PicoBlaze Tools[8] (under construction) |

# 2.1.1. Inhalt

Folgende Themen werden behandelt:

- Digitaltechnik:
  - Zahlendarstellung
  - Boolsche Logik
- Mikroprozessortechnik:
  - CPU-Architekturen
  - Aufbau des Mikrocontrollers PicoBlaze
  - Instruktionssatz
  - Steuerungen und Regelungen mit Mikrocontrollern

# 2.1.2. Ergänzende Lehrbücher

Heesel, N. und W. Reichstein: Mikrocontroller Praxis.
Vieweg, 1996

[3] https://elli.hs-bremerhaven.de/
[4] https://elli.hs-bremerhaven.de/
[5] ../Klausur/pdmpss03.pdf
[6] ../Klausur/dmps031.pdf
[7] ../VHDL/DcMot_Poss.pdf
[8] http://www1.hs-bremerhaven.de/kmueller/picoblazeTools/

Limbach, S.: Kompaktkurs Mikrocontroller.
Vieweg, 2002

Raisonance 80C51 and XA Development Tools Manual.
Raisonance S.A., 2000

K. Urbanski u. R. Woitowitz: Digitaltechnik.
Springer, 2000

J. Wakerly: Digital Design: Principles and Practices.
Prentice-Hall, 1999

Xilinx Vivado Users's Guide.
Xilinx Corp., 2016

# 2.2. Wahlveranstaltungen im Sommersemester 2021 von Kai Müller (optional courses)

Das Modul "ET-DMT" (Digital- und Mikroprozessortechnik) kann als Wahlpflichtmodul von allen technischen Studiengängen belegt werden. Beide Module sind empfohlene Voraussetzungen für den Master *ESD*.

Depending on the audience the course language will be english or german.

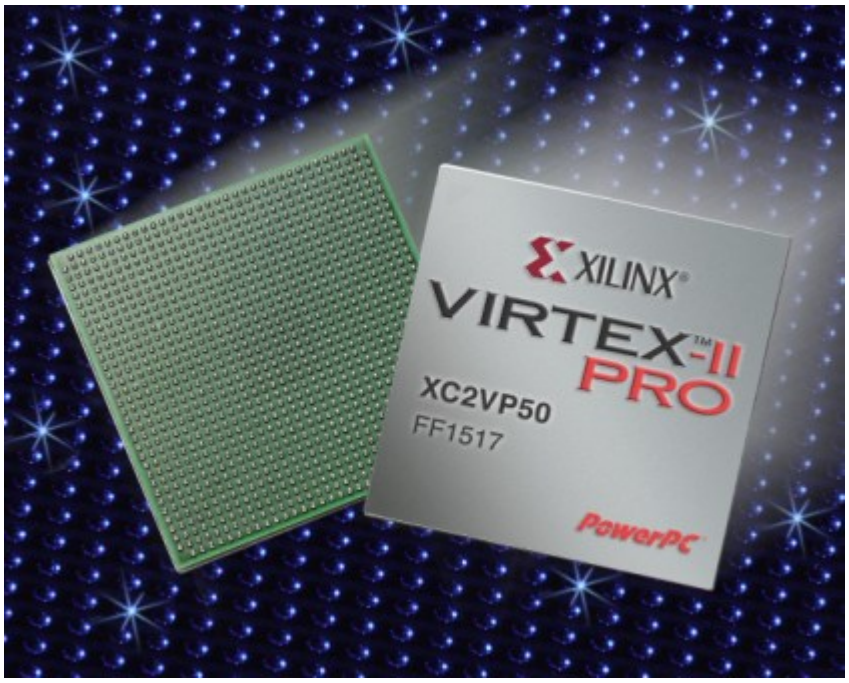
Die Wahlveranstaltungen sind für alle Studierenden der technischen Fächer geeignet.

# 3

# Graduate Courses of Kai Mueller

[modules for *master* programs]

## 3.1. Digital Systems / VHDL [ET-DTV / ESD1]



© Xilinx[1]

**Table 3.1. Organization Digital Systems / VHDL**

| | |
|---|---|
| *NEWS* | *On-line Classes!*<br><br>*Please register on elli[2] (unter ESD S21 -> ET-DTV Digital Systems/VHDL S21)*<br><br>Classes and labs of this module will take place in the first half of this summer term (class 4 hours, lab 4 hours). It ends on May, 19 (estimated).<br><br>This module is required for SY-SOC (System-on-Chip Design) which starts on May 24 (estimated). |

[1] http://www.xilinx.com/
[2] https://elli.hs-bremerhaven.de/

| | |
|---|---|
| Study Program | Master Embedded Systems Design [ESD1] |
| Course Language | English |
| Module Description | ET-DTV[3] |
| Exam (1.) | - no exam - |
| Exam (2.) | t.b.s. |
| Credits | 5 |
| Module Type | class: 4 hours/week<br><br>lab: 4 hours/week<br><br>first half of summer term |
| Lecturer | Prof. Dr. Kai Mueller |
| Start of Course | Monday, April 12, 2021, 08:30h, *Cisco WebEX (online)* |
| End of Course | Wednesday, May 19, 2021 (lab) |
| Class/Lab Dates | Class #1: Monday, block 1, (08:30h)<br><br>Class #2: Monday, block 2, (10:15h)<br><br>==> *Lab requires to have a paper printout of the lab doc when attending the lab.*<br><br>Lab #1: Tuesday, block 4 (14:15h)<br><br>Lab #2: Tuesday, block 5 (16:00h |
| Documents | ==> Course documentation on elli[4]<br><br>*Additional Docs:*<br><br>[ESD Sample Design][5]<br><br>[FPGA Technology Basics][6] (new) This material has copyright by © Xilinx University Program, © University of Strathclyde and © Steepest Ascend Ltd, 2012<br><br>[VHDL Quick Reference][7] © Qualis Corp.<br><br>[IEEE Standard Logic Quick Reference][8] © Qualis Corp. |
| Mandatory Lab Reports & Deadlines | For *deadlines* see lab group participants...<br><br>*Report #1: Moving Light (Sequential Logic Introduction)*<br><br>*Report #2: Timed state machine (Traffic Light Controller)*<br><br>*Report #3: Function Generator with DAC*<br><br>All designs must be synthesizable. Therefore the Synthesis Script must be part of the report (see below). Every report must contain names and matriculation numbers - group reports up to 3 students are allowed. |

[3] http://www1.hs-bremerhaven.de/kmueller/esd/esdmc/modules/ET-DTV_e.html
[4] https://elli.hs-bremerhaven.de/
[5] ../Skript/ESDsdex.pdf
[6] ../VHDL/FPGA_Techn.pdf
[7] ../VHDL/vhdlref.pdf
[8] ../VHDL/1164qrc.pdf

| | |
|---|---|
| | Started : "Synthesize - XST".<br>Running xst...<br>Command Line: xst -intstyle ise -ifn "C:/Mue/xdev14/spirxtx/spirxtx.x<br>Reading design: spirxtx.prj<br><br>=========<br>* HDL Parsing *<br>=========<br>Parsing VHDL file "C:\Mue\xdev14\spirxtx\spitx.vhd" into library wo<br>Parsing entity <spitx>.<br>Parsing architecture <Behavioral> of entity <spitx>.<br>Parsing VHDL file "C:\Mue\xdev14\spirxtx\spirx.vhd" into library wo<br>Parsing entity <spirx>.<br>Parsing architecture <Behavioral> of entity <spirx>.<br>Parsing VHDL file "C:\Mue\xdev14\spirxtx\spirxtx.vhd" into library v<br>Parsing entity <spirxtx>.<br>Parsing architecture <Behavioral> of entity <spirxtx>.<br><br>=========<br>* HDL Elaboration *<br>=========<br><br>etc...<br><br>Timing Summary:<br>---------<br>Speed Grade: -3<br><br>Minimum period: 2.728ns (Maximum Frequency: 366.623MHz)<br>Minimum input arrival time before clock: 3.567ns<br>Maximum output required time after clock: 3.634ns<br>Maximum combinational path delay: No path found<br><br>=========<br><br>Process "Synthesize - XST" completed successfully |
| Examination Topics and Sample Test<br>  | Test question are selected from the topics below:<br><br>[Topics ET-DTV][9]<br><br>Sample Test:<br><br>==>> [ET-DTV Sample Test][10]<br><br>Solutions:<br><br>==>> [Sample Test Solutions][11] |

# 3.1.1. Course contents

- Digital Systems
  - Number Systems / Codes

[9] ../Klausur/etdtv_topics.pdf
[10] ../Klausur/etdtv_st.pdf
[11] ../Klausur/etdtv_stsoln.pdf

  - Combinational Logic
  - Sequential Systems, State Machines
  - Microprocessors, RISC and CISC Architectures
  - Busses, Ports
  - CPLDs, FPGAs
- VHDL
  - Simulation and Verification of Digital Systems
  - Design of Combinational and Sequential Systems
  - Libraries
  - Intellectual Properties

# 3.1.2. Complimentary Documentation

K. Urbanski u. R. Woitowitz: Digitaltechnik.
Springer, 2000

J. Wakerly: Digital Design: Principles and Practices.
Prentice-Hall, 1999

J. Reichardt, B. Schwarz: VHDL-Synthese.
Oldenbourg, 2001

S. Yalamanchili: VHDL Starter's Guide.
Prentice-Hall, 1998

P. J. Ashenden: The Designer's Guide to VHDL.
Elsevier/Morgan Kaufmann, 2008

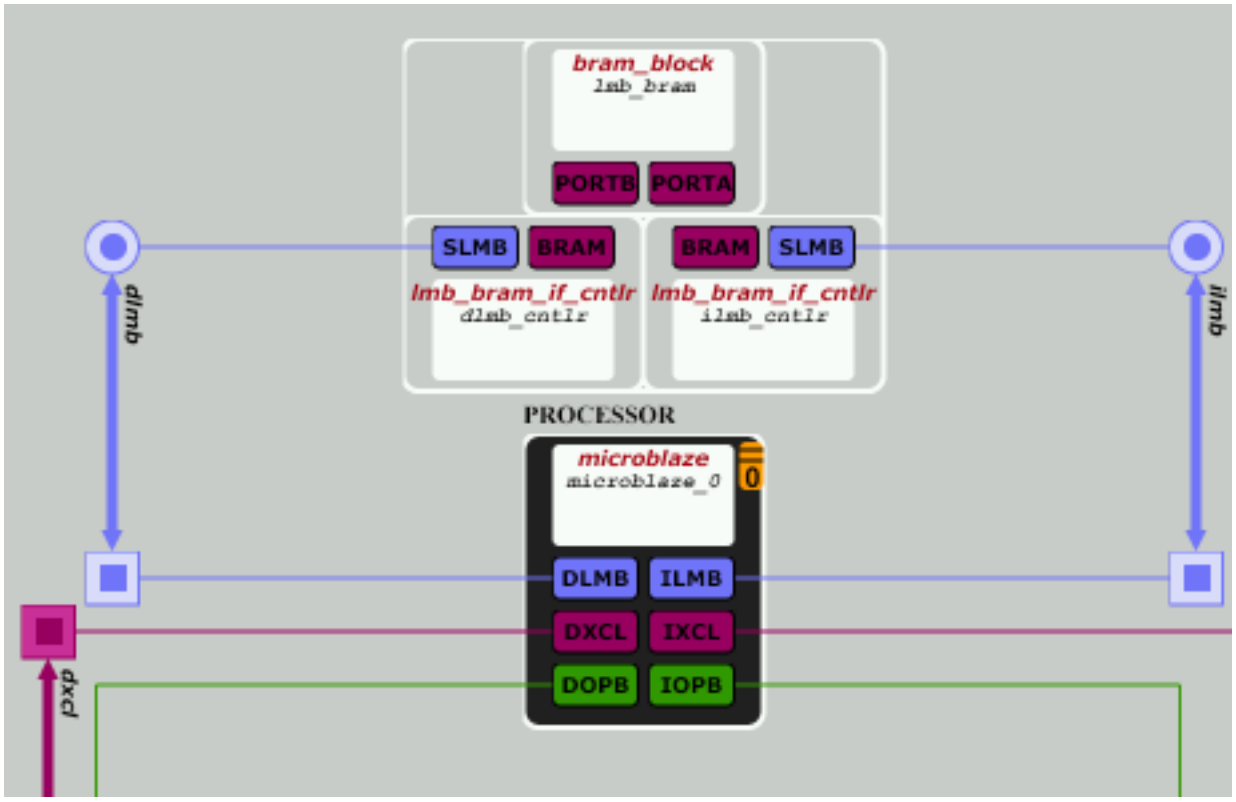
V. A. Pedroni: Circuit Design and Simulation with VHDL.
MIT Press, 2010

R. Lipsett, C. Schaefer and C. Ussery: VHDL: Hardware Description and Design.
Kluwer Academic Publishers, 1990

Xilinx Vivado Users's Guide.
Xilinx Corp., 2019

Modelsim User's Guide.
Mentor Graphics, 2010

# 3.2. System-on-Chip Design [SY-SOC / ESD1]




© Xilinx[12]

**Table 3.2. Organization System-on-Chip Design**

| | |
|---|---|
| *NEWS* | *Start of course is Monday, May 24, 08:30h, Webex online*<br><br>The module ET-DTV (Digital Systems / VHDL) is required to take this course. |
| Study Program | Master Embedded Systems Design [ESD1] |
| Course Language | English |
| Module Description | SY-SOC[13] |
| Exam (1.) | - no exam - |
| Exam (2.) | t.b.s. |
| Credits | 5 |
| Module Type | class: 4 hours/week<br><br>lab: 4 hours/week<br><br>second half of summer term |
| Lecturer | Prof. Dr. Kai Mueller |
| Start of Course | Monday, May 24, 2021, *08:30h* |
| End of Course | Wednesday, July 14, 2021 (lab) |
| Class/Lab Dates | Class #1: Monday, block 1, (08:30h)<br><br>Class #2: Monday, block 2, (10:15h) |

[12] http://www.xilinx.com/
[13] http://www1.hs-bremerhaven.de/kmueller/esd/esdmc/modules/SY-SOC_e.html

| | |
|---|---|
| | ==> *Lab requires to have a paper printout of the lab doc when attending the lab.*<br><br>Lab #1: Tuesday, block 4 (14:15h)<br><br>Lab #2: Tuesday, block 5 (16:00h |
| Mandatory Lab Reports | *Report #1: Discrete PI Controller (PicoBlaze)*<br><br>*Report #2: Hardware accelerated DSP (Zynq)*<br><br>The design must be fully synthesized. Every report must contain name and matriculation number. |
| Documents | ==> Course documentation on elli[14]<br><br>*Additional Docs:*<br><br>[PicoBlaze User Guide][15] © Xilinx Corp.<br><br>*[PicoBlaze Instruction Set Summary][16] © Xilinx Corp. (very important)*<br><br>[PicoBlaze Instruction Set Reference][17] © Xilinx Corp. (not so important) |
| Examination Topics and Sample Test<br>  | Test question are selected from the topics below:<br><br>[Topics ET-SOC][18]<br><br>Sample Test:<br><br>==>> [SY-SOC Sample Test][19]<br><br>Solutions:<br><br>==>> [Sample Test Solutions][20] |

# 3.2.1. Course contents

- Embedded Processors
  - Microprocessor Cores in FPGAs, 8 Bits / 32 Bits
  - Software Development of Embedded CPUs
  - Memory Interface / Memory Controllers
  - Busses
  - Interrupts
  - Real-time Scheduler, Operating Systems
- Periphery

[14] https://elli.hs-bremerhaven.de/
[15] ../VHDL/ug129.pdf
[16] ../VHDL/PB_Instr_Sum.pdf
[17] ../VHDL/PB_Instr_Ref.pdf
[18] ../Klausur/etsoc_topics.pdf
[19] ../Klausur/sysoc_st.pdf
[20] ../Klausur/sysoc_stsoln.pdf

  - A/D- and D/A-converters
  - Serial Busses
  - Ethernet and Real-time Ethernet
- Sample applications
  - Simple Industrial Control System
  - Simple Medical Device
  - Measurement System

# 3.2.2. Complimentary Documentation

J. Wakerly: Digital Design: Principles and Practices.
Prentice-Hall, 1999

Pong P. Chu: FPGA Prototyping By VHDL Examples
(Xilinx Spartan-3 Version)
Wiley Interscience, 2008

R. Reis, M. Lubaszewski, J.A.G. Jess: Design of Systems on a Chip: Design and Test
Springer 2010

B.M. Al-Hashimi: System-on-Chip: Next Generation Electronics (Circuits, Devices and Systems)
Instit. of Eng. and Technology, 2006

Xilinx PicoBlaze™ Users's Guide.
Xilinx Corp., 2014

Xilinx MicroBlaze™ Users's Guide.
Xilinx Corp., 2014

Modelsim User's Guide.
Mentor Graphics, 2012

# 4 Bachelor / Master Thesis

Bachelorarbeiten bzw. Master Thesis im Bereich Automatisierungstechnik, Regelungstechnik, Messtechnik oder Embedded Systems können können am IAE oder in der Industrie angefertigt weden.

*Angebote:*

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Anschrift:

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Institut für Automatisierungs- und Elektrotechnik (IAE)
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